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B. E. (Fourth Semester) Examination, April-May 2020

(New Scheme)

(IT Branch)

COMPUTER ORGANIZATION and ARCHITECTURE

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

***Note** : Attempt all questions. Part (a) of each question is compulsory. Attempt any **two** parts from (b), (c), (d) of each question. The figures in the right-hand margin indicate marks.*

Unit-I

1. (a) Explain the fetch decode execute cycle. 2

(b) Explain the different types of addressing modes with examples. 7

(c) What do you mean by Bus inter connection and also explain types of Bus inter connection. 7

(d) What is stack organization and also explain the instruction format? 7

Unit-II

2. (a) Write the difference between underflow and over-flow. 2

(b) Explain floating point representation and draw the flow chart for division. 7

(c) Write short note on Booth multiplication algorithm with an examples. 7

(d) Write short notes on Hardware algorithm and Binary multiplication. 7

Unit-III

3. (a) What is Control Memory? 2

(b) Explain micro-programmed control unit with also write its advantages and disadvantages. 7

(c) Explain hardwired control unit with also write its advantages and disadvantages. 7

(d) Explain address sequencing in brief. 7

Unit-IV

4. (a) Explain memory hierarchy. 2

(b) Write the difference between RAM and ROM chips and also explain the memory address mapping. 7

(c) What is Cache Memory also write the issues of cache coherance? 7

(d) (i) How many 128 × 8 RAM chips are needed to provide a memory capacity of 2098 bytes?

(ii) How many lines of the address bus must be used to access 2098 bytes of memory? How many of these lines will be common to all chips?

(iii) How many lines must be decoded for chip select? Specify the size of the decodens. 7

Unit-V

5. (a) Explain input output interface. 2

(b) What is pipeling and also explain linear and non linear pipeline? 7

(c) What is input output processor and also explain the data communication between CPU and Input Output? 7

(d) Explain programmed I/O, Interrupt driven I/O and DMA. 7